

United States Court of Appeals for the Federal Circuit

Micron Technology, Inc.

Appellant,

v.

Director of the U.S. Patent &
Trademark Office

Appellee.

SOLICITOR

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U.S. PATENT & TRADEMARK OFFICE

Micron Technology, Inc. hereby appeals the court for review of the decision of the Board of Patent Appeals and Interferences in Appeal No. 2005-1576, Application No. 09/885,217, entered on 31 October 2005.

Respectfully submitted,



Edward L. Pencoske
Jones Day
500 Grant Street, Suit 3100
Pittsburgh, PA 15219-2502
(412) 394-9531
Attorney for Applicants

Dated: 29 December 2005

The opinion in support of the decision being entered today was not written publication and is not binding precedent of the Board.

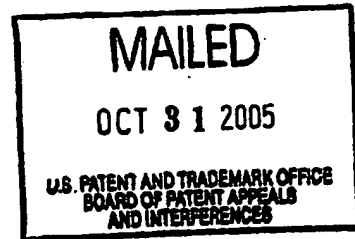
UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte BRENT KEETH
and LAYNE G. BUNKER

Appeal No. 2005-1576
Application No. 09/885,217

ON BRIEF



Before RUGGIERO, GROSS, and BARRY, Administrative Patent Judges.
RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 223, 225, 228-237, 247-250, 496, and 499-515.

The claimed invention relates to a voltage reference circuit for supplying a reference voltage in which an active reference circuit receives an external voltage and produces a reference signal having a desired relationship with the external voltage. The active reference circuit includes a current source utilizing a current mirror to provide current to a diode stack having an adjustable impedance. Further included is a unity gain amplifier

acting in response to the reference signal, which is dependent on the external voltage, for producing the reference voltage.

Claim 223 is illustrative of the invention and reads as follows:

223. A voltage reference circuit responsive to an external voltage for supplying a reference voltage, comprising:

an active reference circuit for receiving the external voltage and for producing a reference signal having a desired relationship with the external voltage, said active reference circuit comprising a current source utilizing a current mirror for providing current to a diode stack having an adjustable impedance, wherein said reference signal is dependent upon said external voltage; and

a unity gain amplifier responsive to said reference signal for producing the reference voltage.

The Examiner relies on the following prior art:

Hayakawa et al. (Hayakawa)	5,184,031	Feb. 02, 1993
Park	5,448,199	Sep. 05, 1995
Morishita et al. (Morishita)	5,757,175	May 26, 1998 (filed Jan. 13, 1997)
Zarrabian et al. (Zarrabian)	5,838,076	Nov. 17, 1998 (filed Nov. 21, 1996)
Tsay et al. (Tsay)	6,127,881	Oct. 03, 2000 (filed May 31, 1994)

Claims 223 and 511 stand finally rejected under 35 U.S.C. § 102(e) as being anticipated by Morishita. Claims 225, 496, 499, 500, and 514 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Morishita in view of Zarrabian.

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Claims 228-230 and 501-503 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Morishita in view of Park. Claims 231, 504, 512, and 515 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsay in view of Morishita. Claims 232, 233, 505, and 506 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayakawa in view of Tsay and Morishita. Claims 234-237, 247-250, 507-510, and 513 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayakawa in view of Tsay, Morishita, and Park.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Briefs¹ and Answer for their respective details.

OPINION

We have carefully considered the subject matter on appeal, the rejections advanced by the Examiner, the arguments in support of the rejections, and the evidence of anticipation and obviousness relied upon by the Examiner as support for the

¹The Appeal Brief was filed March 18, 2004. In response to the Examiner's Answer mailed June 3, 2004, a Reply Brief was filed July 19, 2004, which was acknowledged and entered by the Examiner as indicated in the communication mailed November 5, 2004.

rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellants' arguments set forth in the Briefs along with the Examiner's rationale in support of the rejections and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the disclosure of Morishita fully meets the invention as recited in claims 223 and 511. In addition, we are of the opinion that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 225 and 228-237, 247-250, 496, 499-510, and 512-515. Accordingly, we affirm.

At the outset, we note that Appellants indicate (Brief, page 3) that, for purposes of this appeal, all claims will stand or fall together. Consistent with this indication, Appellants' arguments in the Brief are directed solely to features which are set forth in independent claim 223. Accordingly, we will select independent claim 223 as the representative claim for all the claims on appeal, and claims 225, 228-237, 247-250, 496, and 499-515 will stand or fall with claim 223. Note In re King, 801 F.2d

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1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983).

We note that anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

At pages 3, 4, 10, and 11 of the Answer, the Examiner indicates how the various limitations in representative claim 223 are read on the disclosure of Morishita. In particular, the Examiner directs attention to the illustrations in Figures 17-19 of Morishita along with the accompanying description beginning at column 1, line 66 of Morishita.

In our view, the Examiner's analysis is sufficiently reasonable that we find that the Examiner has at least satisfied the burden of presenting a prima facie case of anticipation. The burden is, therefore, upon Appellants to come forward with

evidence and/or arguments which persuasively rebut the Examiner's prima facie case. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived [see 37 CFR § 41.37(c)(1)(vii)].

Appellants' arguments in response assert that the Examiner has not shown how each of the claimed features are present in the disclosure of Morishita so as to establish a case of anticipation. In particular, Appellants contend that, in contrast to the claimed invention, "Morishita fails to teach a voltage reference circuit that includes a unity gain amplifier for producing a reference voltage in response to a reference signal." (Brief, page 4).

After careful review of the Morishita reference in light of the arguments of record, however, we are in general agreement with the Examiner's position as stated in the Answer. We find no arguments from Appellants that convince us of any error in the Examiner's position which, considering the entire circuitry illustrated in Figure 17 of Morishita as a voltage reference circuit, asserts that the amplifier circuit comprising elements

CMP and DT in Morishita is a unity gain amplifier. We further agree with the Examiner that Morishita's unity gain amplifier produces a reference voltage as claimed since the reference voltage V_{ref} is maintained at the internal power supply voltage INV_{cc} level.

We further find to be unpersuasive Appellants' argument (Reply Brief, page 2) that, unlike the claimed invention, the reference signal in Morishita does not have a desired relationship with the external voltage. In support of this contention, Appellants rely on certain portions of Morishita which, in their view, suggest that no reference voltage is produced until the external voltage exceeds a predetermined voltage level.

It is our opinion, however, that even assuming, arguendo, that Appellants' characterization of the operation of the circuitry of Morishita is correct, such circuit operation in fact satisfies the language of claim 223. In other words, the fact alone that a reference voltage in Morishita may not be produced until an external voltage exceeds a prescribed level establishes, in our view, a desired relationship with such external voltage.

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Similarly, the reliance on the attaining of a voltage level by the external voltage in Morishita before a reference voltage is produced makes Morishita's reference voltage dependent on the external voltage as claimed.

In view of the above discussion, since the Examiner's prima facie case of anticipation has not been overcome by any convincing arguments from Appellants, the Examiner's 35 U.S.C. § 102(e) rejection of representative claim 223, as well as claims 225, 228-237, 247-250, 496, and 499-515 which fall with claim 223, is sustained. Therefore, the decision of the Examiner rejecting claims 223, 225, 228-237, 247-250, 496, and 499-515 is affirmed.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(1)(iv) (effective September 13, 2004).

AFFIRMED

Joseph F. Ruggiero
JOSEPH F. RUGGIERO
Administrative Patent Judge

Anita Pelman Gross
ANITA PELLMAN GROSS
Administrative Patent Judge

BOARD OF PATENT
APPEALS
AND
INTERFERENCES

LANCIE LEONARD BARRY
Administrative Patent Judge

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